WHAT IS CLAIMED IS:

1. A signal processing apparatus, comprising:

first computing means and second computing means operating independent of each other; and

interface means interconnecting said first computing means and said second computing means,

wherein upon power-up of said signal processing apparatus, said first computing means transfers data to said second computing means by way of said interface means, whereupon signal processing in an ordinary operation mode is executed.

2. A signal processing apparatus according to claim 1,

wherein said first computing means transfers the data required by said second computing means.

3. A signal processing apparatus according to claim 1, further comprising:

data rewritable nonvolatile memory means,

said nonvolatile memory means having a program memory map corresponding to said first computing means,

wherein a run start address of said second computing means, a program data size and program data therefor are arrayed in a parameter table area of said program memory map corresponding to said first computing unit.

4. A signal processing apparatus according to claim 1,

wherein said interface means includes a serial interface and general-purpose signaling means.

5. A signal processing apparatus according to claim 4,

wherein said first and second computing means are so arranged that upon power-up of said signal processing apparatus, said first computing means firstly transfers data of a predetermined unitary amount to said second computing means via said serial interface, while said second computing means inverts polarity of said general-purpose signaling means after lapse of a predetermined time since the end of the first data transfer, and when said first computing means starts again the data transfer, said second computing means inverts again the polarity of said general-purpose signaling means, to thereby carry out the data transfer upon power-up of said signal processing apparatus through repetition of the data transfer and the polarity inversion of said general-purpose signaling means, whereupon signal processing in an ordinary operation mode is executed.

6. A signal processing apparatus according to claim 1, further comprising:

read-only memory means incorporated in said second computing means; and

volatile memory means incorporated in said second computing means or connected thereto by way of an address bus and a data bus.

7. A signal processing apparatus, comprising:

a first computing unit and a second computing unit operating independent of each other; and

an interface interconnecting said first computing unit and said second computing unit,

wherein upon power-up of said signal processing apparatus, said first computing unit transfers data to said second computing unit by way of said interface whereupon signal processing in an ordinary operation mode is executed.

8. A signal processing apparatus according to claim 7,

wherein said first computing unit transfers the data required by said second computing unit.

9. A signal processing apparatus according to claim 7, further comprising:

a data rewritable nonvolatile memory,

said nonvolatile memory having a program memory map corresponding to said first computing unit,

wherein a run start address of said second computing unit, a program data size and program data therefor are arrayed in a parameter table area of said program memory map corresponding to said first computing unit.

10. A signal processing apparatus according to claim 7,

wherein said interface includes a serial interface and a general-purpose signal line.

11. A signal processing apparatus according to claim 10,

wherein said first and second computing units are so arranged that upon power-up of said signal processing apparatus, said first computing unit firstly transfers data of a predetermined unitary amount to said second computing unit via said serial interface, while said second computing unit inverts polarity of said general-purpose signal line after lapse of a predetermined time since the end of the first data transfer, and when said first computing unit starts again the data transfer, said second computing unit inverts again the polarity of said general-purpose signal line, to thereby carry out the data transfer upon power-up of said signal processing apparatus through repetition of the data transfer and the polarity inversion of said general-purpose signal line, whereupon signal processing in an ordinary operation mode is executed.

12. A signal processing apparatus according to claim 7, further comprising:

a read-only memory incorporated in said second computing unit; and

a volatile memory incorporated in said second computing unit or connected thereto by way of an address bus and a data bus.